

REFERENCE PHASE LOCKED TRANSLATOR

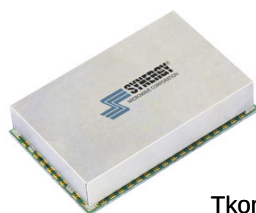
SURFACE MOUNT MODEL: FXLNS-1000

FIXED FREQUENCY

1000 MHz

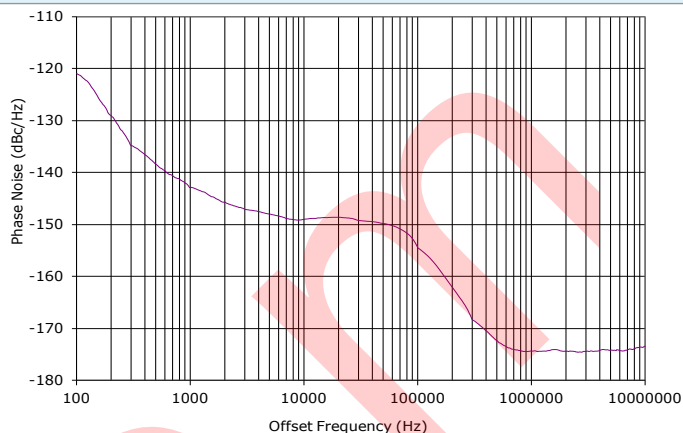
FEATURES:

- ▶ Ultra-Low Phase Noise
- ▶ No Programming Required



Tkom*

Phase Noise (Measured with Agilent E5052A or R&S FSUP-26/50)



SPECIFICATIONS (Rev. A 04/08/13)

Frequency	1000 MHz						
Reference Input Frequency	100 MHz ¹						
Reference Input Power	13 ±3 dBm						
Bias Voltage	<table> <tr> <th>VCC</th><th>VDC @ I</th></tr> <tr> <td>VCC1</td><td>+5 VDC @ 200 mA (Max.)</td></tr> <tr> <td>VCC2</td><td>+12 VDC @ 45 mA (Max.)</td></tr> </table>	VCC	VDC @ I	VCC1	+5 VDC @ 200 mA (Max.)	VCC2	+12 VDC @ 45 mA (Max.)
VCC	VDC @ I						
VCC1	+5 VDC @ 200 mA (Max.)						
VCC2	+12 VDC @ 45 mA (Max.)						
Output Power	-2 dBm (Min.)						
Spurious Suppression	55 dB (Typ.)						
Harmonic Suppression	35 dB (Typ.)						
Output Impedance	50 Ohms (Nom.)						
Lock Detect Indicator	CMOS 3.3 V						

¹ External 100 MHz reference sources should have phase noise better than -143 dBc/Hz @ 100 Hz offset to achieve published specifications.

Patent : <http://www.synergymwave.com/patents>

Typical Phase Noise

Offset	Phase Noise
@ 100 Hz	-120 dBc/Hz
@ 1 kHz	-140 dBc/Hz
@ 10 kHz	-149 dBc/Hz
@ 100 kHz	-154 dBc/Hz
@ 1 MHz	-174 dBc/Hz

Operating Temperature Range

-20 to +70 °C

Absolute Maximum Ratings

Storage Temp. Range	-40 to +85 °C
Bias Voltage VCC1 (+5 V)	+6.0 V
Bias Voltage VCC2 (+12 V)	+13.0 V
DC Bias Voltage applied to RF output	±25 V

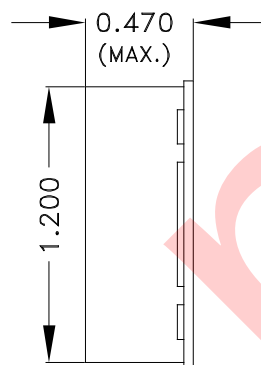
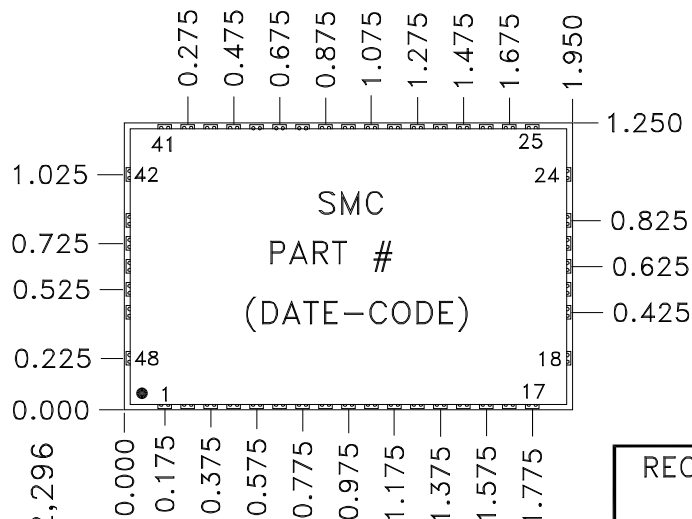
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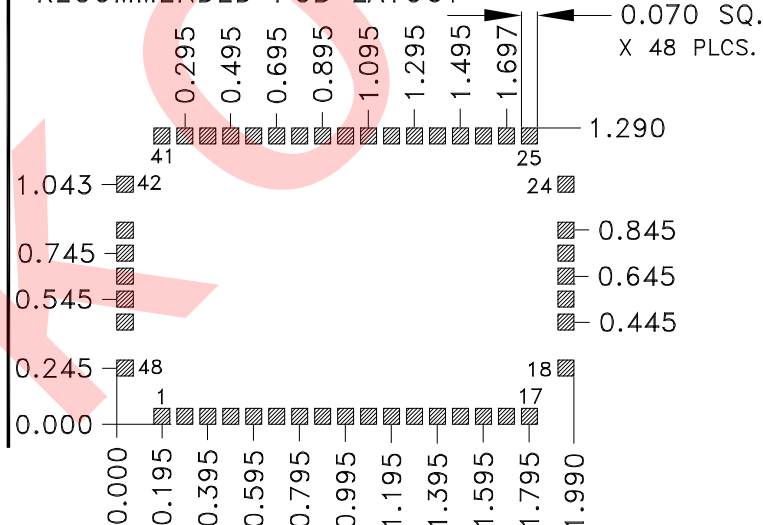
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1000 MHz

Package # 344



RECOMMENDED PCB LAYOUT



TOLERANCES ON THREE
DECIMAL PLACES = ± 0.015

PACKAGE MOUNTING: SEE APPLICATION NOTE AN7200 & AN7300

PORT CONFIGURATION

Pin 3 - VCC 1 ***
Pin 6 - RF OUT
Pin 8 - NC
Pin 9 - NC
Pin 10 - NC
Pin 11 - NC
Pin 12 - NC
Pin 13 - NC
Pin 14 - Lock Detect (LD) **
Pin 15, 16 - NC

Pin 18,19,20,21 - NC
Pin 22 - Reference In
Pin 27 - VCC 1 ***
Pin 28 - VCC 2
Pin 30,31 - NC
Pin 35 - NC
Pin 39 - VCC 1 ***
Pin 40 - NC
Pin 44 - VCC 2
Pin 43,45 - NC

All others - Ground
NC - No connection

* Connect together externally and bypass with shunt 10 uF, 35 V capacitor to ground.

** Positive CMOS levels (unbuffered 3.3 VDC)

*** Connect together externally and bypass with shunt 10uF, 10 V capacitor to ground

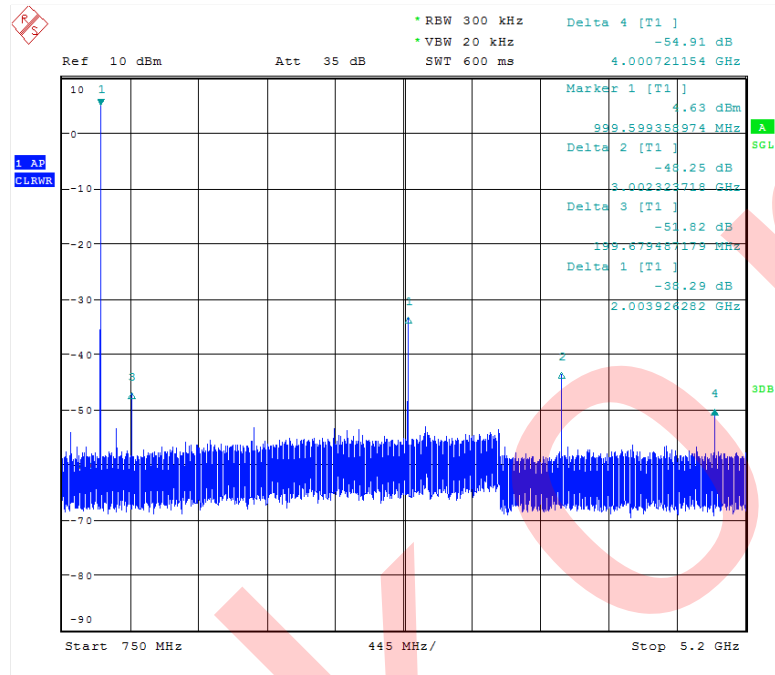
REFERENCE PHASE LOCKED TRANSLATOR SURFACE MOUNT MODEL: FXLNS-1000

FIXED FREQUENCY

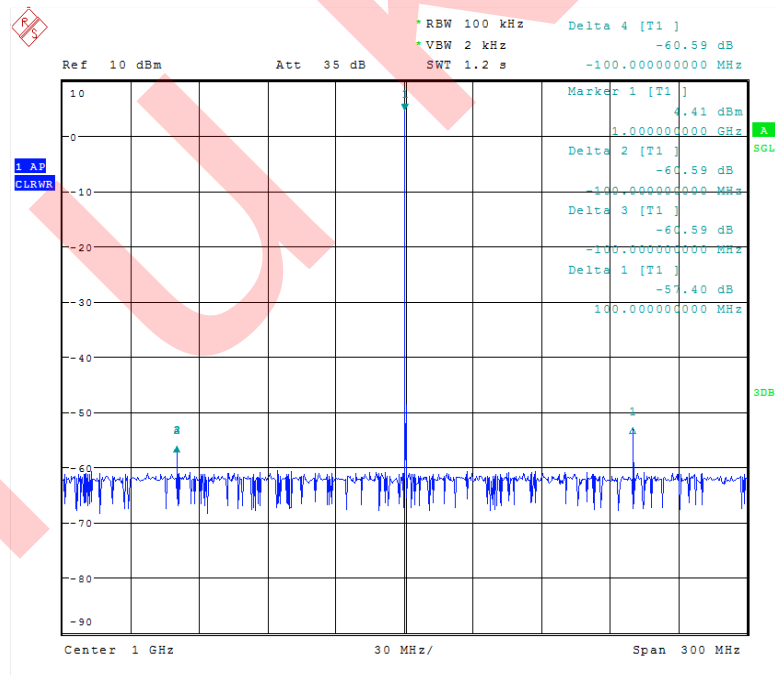
1000 MHz

HARMONIC SUPPRESSION

@ 25 °C



WIDE BAND SFDR



PERFORMANCE PLOTS

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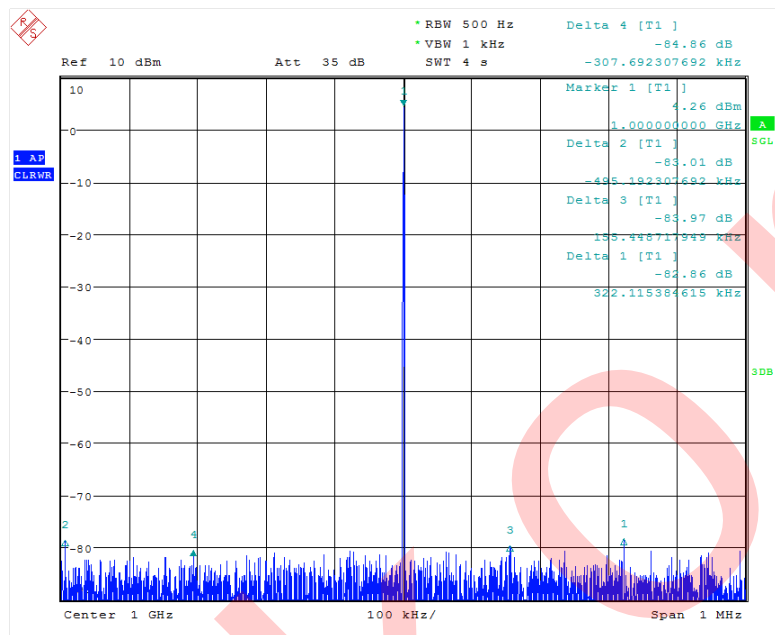
SURFACE MOUNT MODEL: FXLNS-1000

FIXED FREQUENCY

1000 MHz

NARROW BAND SFDR

@ 25 °C



PERFORMANCE PLOTS